REMARKS

By this preliminary amendment, claims 1-13, 17 and 18 are amended, and claims 14-16 are cancelled without prejudice. Appropriate support for the claim amendment can be found at least in Fig. 1 and page 12, lines 3-16. Claims 1-13, 17 and 18 are now active for examination. The specification is amended to add priority information, and Fig. 1 is amended to add a --Prior Art-- legend, and Fig. 7 is amended to add descriptions for items 10-13 and 23. Appropriate support for the drawing amendment can be found in, for example, page 19, last paragraph through page 20, second paragraph. No new matter is added. Entry of this preliminary amendment is respectfully requested.

Claim 1, as amended, describes a control apparatus that includes a control means, a system controller, a first memory, a second memory, and a writing means for writing data in the second memory. The control means is configured to output a first address to one of the first and second memories, and to operate in accordance with program data output from the first selection means; and the system controller is configured to output program data to the writing means and a second address for the second memory when the control means is operating in accordance with the data program from the first memory. Two selection means are provided: a first selection means for selectively outputting an output from one of the first and second memories, and a second selection means for selectively outputting an address for the second memory from one of the control means and the system controller. *The first selection means is configured to select the output from one of the first and second memories in accordance with the first address, and the second selection means is configured to select the second address form the system controller when the control means is operating in accordance with the date program from the first memory.* The writing means enables data to be written in the second memory when the control means is

operating in accordance with the program data from the first memory. Claims 3 and 13 also include, among other things, descriptions comparable to those of claim 1. Appropriate support for the amendment can be found in, for example, item 9 of Fig. 1 and page 12, lines 3-16 of the specification.

Thus, the control apparatus of the claims uses an additional system controller and two selection means to assist the downloading process and reduce the workload of the control means, such that the control means can perform other functions when data is written into the second memory.

It is respectfully submitted that the features described in claims 1, 3 and 13 are not taught in the documents and/or patents made of record in the parent of this application. Specifically, these features cannot be found in Tateishi (EP 0653698 A1) or Azuma (JP2000242598A), two documents cited to reject claims in the parent of this application.

Tateishi is related to a magnetic disk controller having a CPU, a ROM and a RAM. The CPU can access data from either the ROM or the RAM. The magnetic disk controller is coupled to a host processor via a host interface. Although Tateishi discusses accessing data from two memory devices, Tateishi does not describe using two selection means to select output from one of the memories in accordance with an address issued by the CPU, and to select a second address issued by a system controller to be output to the RAM. Therefore, Tateishi fails to teach "a first selection means for selectively outputting an output from one of the first and second memories; the first selection means selecting the output from one of the first and second memories in accordance with the first address;...and a second selection means for selectively outputting an address for the second memory from one of the control means and the system controller; the second selection means selecting the second address form the system controller when the control

means is operating in accordance with the data program from the first memory," as required by claim 1, 3 and 13.

Azuma also fails to teach these features. Azuma describes a host system 2 that includes a CPU 14, a RAM 3 and a ROM 20. The host system connects to EEPROMs 17a, 17c and a disk drive B23 via a bus. The CPU 14 transfers firmware data from EEPROM 17a to the RAM 3, and then transfers the data from RAM 3 to disk drive B23 and EEPROM 17c. Nowhere does Azuma describe the use of two selection means for selectively outputting an output from one of the EEPROMs, and for selectively outputting an address to EEPROM 17c from the CPU or other controllers. Therefore, Azuma also fails to disclose "a first selection means for selectively outputting an output from one of the first and second memories; the first selection means selecting the output from one of the first and second memories in accordance with the first address;...and a second selection means for selectively outputting an address for the second memory from one of the control means and the system controller; the second selection means selecting the second address form the system controller when the control means is operating in accordance with the data program from the first memory," as described in claims 1, 3 and 13.

Other documents and/or patents made of record in the parent application do not alleviate these deficiencies. Thus, Tateishi and Azuma, either individually or in combination with each other or other documents and/or patents made of record in the parent of this application, do not teach every limitation of claims 1, 3 and 13.

Claims 2, 4-2, 17 and 18, directly or indirectly, depend on claims 1, 3 and 13, respectively. Therefore, claims 2, 4-2, 17 and 18 are patentable over the documents and/or patents made of record in the parent application by virtue of their dependency.

It is believed that claims 1-13, 17 and 18 are in condition for allowance. Favorable consideration is respectfully requested.

Respectfully submitted,

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